Amendments to the Specification:

18 Please replace the second paragraph on page 2 with the following amended paragraph:

IDC-A1,AMD In general, the performance of an electronic device depends not only upon the structure grown or formed on the substrate surface, but also upon the properties of the substrate itself. For example, the doping level in the substrate may affect series resistance and current density distribution if the current flows through the substrate, junction capacitance for junction isolated devices, or latch-up tolerance in devices with parasitic thyristors (such as CMOS ICs). Defect densities are also important, affecting leakage currents and device reliability. In the case of an optical device emitting through the substrate (such as a NECSEL (Novalux® Extended Cavity ~~Side~~ Surface Emitting Laser)), optical absorption in the substrate is also important.

~~Please replace the third paragraph on page 3 with the following amended paragraph:~~

IDC-A2,AMD In the particular case of a NECSEL or bottom emitting VCSEL (Vertical Cavity ~~Side~~ Surface Emitting Laser), the importance of the substrate properties is as follows. The current flowing to the gain region passes through the substrate. High conductivity is required to keep the series resistance low and prevent too much current crowding at the device perimeter. This can be achieved through the use of a heavily doped, thick substrate. On the other hand, optical loss must be kept low and this means a low doping level and thin substrate. A third requirement arises from the need to maintain device operation within specification over its entire lifetime. A key element in achieving this is to keep the defect density in the substrate low. An acceptable trade-off between these three requirements (low resistance, low optical loss and low defect density) is difficult to achieve in commercially available substrate materials.

~~Please replace the paragraph bridging pages 4 and 5 with the following amended paragraph:~~

IDC-A3,AMD,M The active components, electrical contacts etc. are formed on top of the grown semiconductor layer using well-established wafer-scale fabrication techniques. At an appropriate stage during this fabrication, the original substrate material is removed from the whole wafer by any suitable technique (mechanical polishing, chemical etching, chemical-mechanical polishing (CMP), chemical or physical plasma etching etc.) leaving only a sufficient